**IN THE CLAIMS**

Please amend the Claims as follows:

1 (Cancelled).

2 (Cancelled).

3 (Cancelled).

4 (Cancelled).

5 (Cancelled).

6 (Cancelled).

7 (Cancelled).

8 (Cancelled).

9 (Cancelled).

10 (Cancelled).

11 (Cancelled).

12 (Cancelled).

13 (Cancelled).

14 (Cancelled).

15 (Cancelled).

16 (Original). A method of manufacturing a semiconductor package, comprising:

mounting a semiconductor die to a substrate;

electrically connecting the semiconductor die to a circuit pattern of the substrate, wherein the substrate has a plurality of bottom side electrical terminals on a bottom side for providing electrical connection to the semiconductor die;

encapsulating the semiconductor die and at least the top surface of the substrate to form an encapsulation;

ablating via holes through the encapsulation; and

depositing conductive material within the via holes to form a plurality of top-surface terminals on the top surface of the semiconductor package for connecting a piggyback semiconductor package to the semiconductor package.

17 (Original). The method of Claim 16, wherein the ablating is performed by a laser.

18 (Original). The method of Claim 16, wherein the ablating ablates the encapsulant to expose a circuit pattern on the top surface of the substrate, and wherein the depositing generates a via that provides electrical connection from at least one of the plurality of top-surface terminals to the circuit pattern.

19 (Original). The method of Claim 16, wherein the ablating ablates the encapsulant to expose an electrical connection on a top surface of the semiconductor die, and wherein the depositing generates a via that provides electrical connection from at least one of the plurality of top-surface terminals to the electrical connection of the semiconductor die.

20 (Original). The method of Claim 16, wherein the ablating ablates the encapsulant and the substrate, and wherein the depositing generates a via that provides electrical connection from at least one of the plurality of top-surface terminals to a corresponding on of the plurality of bottom side terminals.

21 (New). A method of manufacturing a semiconductor package, comprising:

providing a substrate having at least one circuit pattern and a plurality of electrical terminals on a first side of the substrate;

mounting a semiconductor die to a second side of the substrate;

electrically coupling the semiconductor die to the circuit pattern of the substrate;

encapsulating the semiconductor die and at least the second surface of the substrate;

ablating via holes through the encapsulation by a laser; and

depositing conductive material within the via holes for coupling a second semiconductor package to the semiconductor package.

22 (New). The method of Claim 21, wherein the ablating ablates the encapsulant to expose the circuit pattern on the top surface of the substrate, and wherein the depositing provides electrical connection to the circuit pattern.

23 (New). The method of Claim 21, wherein the ablating ablates the encapsulant to expose an electrical connection on a top surface of the semiconductor die, and wherein the depositing provides electrical connection to at least one electrical connection of the semiconductor die.

24 (New). The method of Claim 21, wherein the ablating ablates the encapsulant and the substrate, and wherein the depositing generates a via that provides electrical connection to a corresponding one of the plurality of electrical terminals on the first side of the substrate.

25 (New). The method of Claim 21, wherein ablating via holes through the encapsulation further comprises ablating conical via holes through the encapsulation.

26 (New). The method of Claim 21, wherein ablating via holes through the encapsulation further comprises ablating cylindrical via holes through the encapsulation.

27 (New). The method of Claim 21, further comprising a plurality of contacts, wherein one contact is coupled to each of the plurality of electrical terminals on a first side of the substrate.

28 (New). The method of Claim 21, wherein electrically coupling the semiconductor die to the circuit pattern of the substrate comprises wirebonding the semiconductor die to the circuit pattern of the substrate.

29 (New). The method of Claim 21, wherein depositing conductive material further comprises depositing one of an electroplated or electro-less plated metal within the via holes.

30 (New). The method of Claim 21, wherein depositing conductive material further comprises depositing a conductive paste within the via holes.

31 (New). The method of Claim 21, wherein depositing conductive material further comprises depositing a solder alloy within the via holes.

32 (New). A method of manufacturing a semiconductor package, comprising:

providing a substrate having circuit patterns and a plurality of electrical terminals on a first side of the substrate;

mounting a semiconductor die to a second side of the substrate;

electrically coupling the semiconductor die to a circuit pattern of the substrate;

encapsulating the semiconductor die and at least the second surface of the substrate;

ablating a plurality of via holes through the encapsulation; and

depositing means within the via holes to form a plurality of terminals on the second surface of the semiconductor package for coupling a second semiconductor package to the semiconductor package.

33 (New). The method of Claim 32, wherein the ablating ablates the encapsulant to expose the circuit pattern on the top surface of the substrate, and wherein the depositing provides electrical connection from at least one of the plurality of terminals to the circuit pattern.

34 (New). The method of Claim 32, wherein the ablating ablates the encapsulant to expose an electrical connection on a top surface of the semiconductor die, and wherein the depositing provides electrical connection from at least one of the terminals to at least one electrical connection of the semiconductor die.

35 (New). The method of Claim 32, wherein the ablating ablates the encapsulant and the substrate, and wherein the depositing generates a via that provides electrical connection from at least one of the plurality of terminals to a corresponding one of the plurality of electrical terminals on the first side of the substrate.